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# Crystalline silicon thin foils: Where crystalline quality meets thin-film processing

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ABSTRACT

Today, c-Si photovoltaic technologies dominate the market, accounting for more than 85% of market share in 2010. A large scientific community made up of academic as well as industrial stakeholders strives to find solutions to improve device efficiencies and to drive down costs. One of the important cost elements of a module is the c-Si wafer itself. This paper discusses the fabrication of a carpet of c-Si foils on glass, either by layer transfer of an epitaxially-grown layer or by bonding of a very thin wafer, and processing this c-Si thin-foil device into a photovoltaic module. This could constitute an advantageous meet-in-the-middle strategy that benefits not only from c-Si material quality but also from thin-film processing developments.

## The best of both worlds

Despite a drastic decrease in silicon feedstock prices, and because of even more aggressive cuts in processing costs, it is estimated that the solar wafer today accounts for ~30–40% of the module cost [1]. Reducing the solar wafer thickness, therefore, carries a very strong leverage factor in cutting down costs. Understandably, therefore, the International Technology Roadmap predicts that the thickness of solar wafers will decrease from ~180µm today to ~100µm in 2020 [2]. But the same publication warns the reader that the technological solution to the processing of wafers thinner than 150µm remains to be found. Any attempt by PV manufacturers to reduce the thickness below 150µm has so far resulted in an increase in breakage of the devices during processing, reducing the production yield and therefore annihilating all potential cost reduction offered by thinner wafers.

> "Any attempt by PV manufacturers to reduce the thickness below 150µm has so far resulted in an increase in breakage."

Meanwhile, the thin-film PV development community has no issues with handling. Module and cell fabrication are non-dissociable since the device is grown directly on the module glass. The challenge of this community is elsewhere: device efficiencies remain lower than for crystalline Si modules. Lower module efficiency immediately translates into an increase in balance-of-system cost, jeopardizing the competitiveness of thin-film systems. In addition to the continuous and aggressive decrease in module production costs, increasing conversion efficiency is perceived today as a strategic way for thin-film PV to improve the chance of catching up with the moving target established by the mainstream technology.

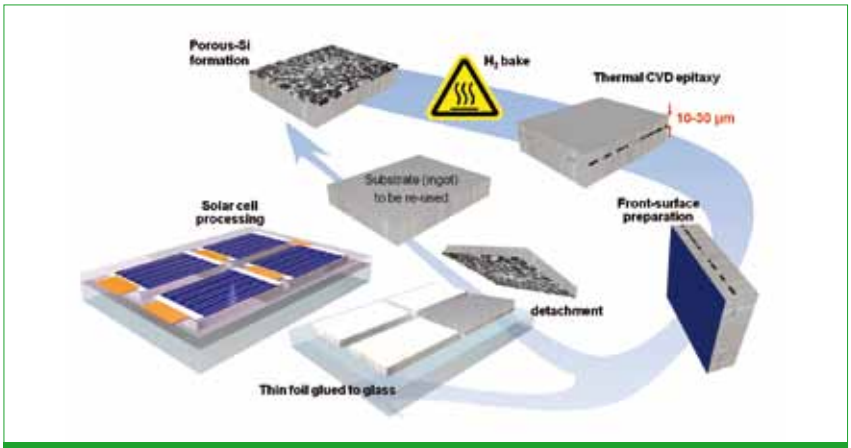


**Figure 1. Schematic of the process proposed for creating an epitaxially-grown crystalline silicon foil on glass.**

The concept described in this article targets a balanced meet-in-the-middle strategy. The intention is to take the best of both worlds: the quality and efficiencies of crystalline silicon devices on the one hand, and low material consumption and parallel and module-level processing of thin-film PV solutions on the other [3]. A c-Si PV device concept compatible with thicknesses below 50µm is proposed; a device concept inspired by thin-film technologies and compatible with efficiencies exceeding 18% is also proposed. These two concepts are in fact only one, consisting of the fabrication of a thin foil of c-Si on glass, followed by its processing, at the module level, into a highly-efficient PV device. The next section describes how the silicon foil can be fabricated on glass, and explains the possibilities offered by the thin-film community for processing it into a PV device. The question of the efficiency potential is finally raised in the last section.

## A crystalline Si foil on glass

The first question that needs to be asked is how to deposit a good-quality c-Si on glass [4]. Direct deposition, in a thin-film-like approach, of a layer of crystalline silicon results in poor electronic properties. It has therefore been proposed to epitaxially grow a monocrystalline Si layer on a monocrystalline seed-substrate and transfer this material to a foreign substrate [5–7]. The method implies the use of a sacrificial weak layer, which can either be an oxide layer [8,9], or be achieved by light-ion implantation [10], or more often by porosification of the parent substrate before growth [6]. In the latter case, as depicted in Fig. 1, a high-quality wafer is first anodized to create a superficial layer of porous Si (PSi); a chemical vapour

deposition (CVD) process deposits a relatively thick (several tens of microns) active layer epitaxially on the wafer, which replicates the initial crystallographic quality of the wafer; the active layer is then detached from the parent wafer and bonded to a foreign sub/superstrate, while the parent wafer is reused. The bonding can be realized with, for instance, a silicone material, specifically tuned to buffer the stress due to the difference in thermal coefficient of expansion between the Si layer and the glass.

The foil quality is of utmost importance and strongly depends on the morphology of the porous layer. The weak layer therefore usually consists of a double layer of high and low porosity [11,12]. The high-porosity layer is tuned to approximately 40–70% porosity to allow easy detachment. The low-porosity layer (15–25%) seeds the epitaxial growth. A high-temperature (>900°C) annealing step is required to close the Si surface before growth. The growth of the active layer provides an elegant way of creating the p-n junction of the device (and potentially also surface fields) directly by epitaxy. This potentially reduces the number of process steps, and facilitates the implementation of advanced emitter profiles [13]. Solar cell efficiencies of up to 19.1% were recently obtained on free-standing foils fabricated on a PSi weak layer, showing the high-material-quality potential of the method [14,15].

In the concept we are proposing the front-surface treatment (texturization, surface passivation, antireflective coating deposition) is performed just before bonding while the foil is still attached to the mother substrate, and the rear side is processed on glass. The thin foil is thus constantly mechanically supported during the process. The porous layer should therefore be strong enough to withstand front-side processing, but weak enough to allow easy detachment after bonding [12].

Standard (180µm-thick) wire-sawn silicon wafers are, in principle, compatible with the process described in this paper. They can be bonded in a carpet-like fashion on a glass plate, creating a layer of crystalline silicon material, which can be further processed into a solar module. Nonetheless, because of the very high contribution of the silicon material to the cost of solar modules today, and since the concept described does not suffer from handling issues during processing, it is desirable to consider much thinner wafers. Multiple-wire saw technology is unlikely to be able to produce wafers thinner than 80–100µm [2,16]. In addition, the kerf (saw cut) has dimensions comparable to the wafer thickness, leading to an intrinsic kerf loss of 40–50%, and up to 70% for wafers < 100µm thick [2,17]. Therefore, in order to get the full benefit of this concept, alternative kerf-free wafering techniques that conserve the material quality have to be developed.

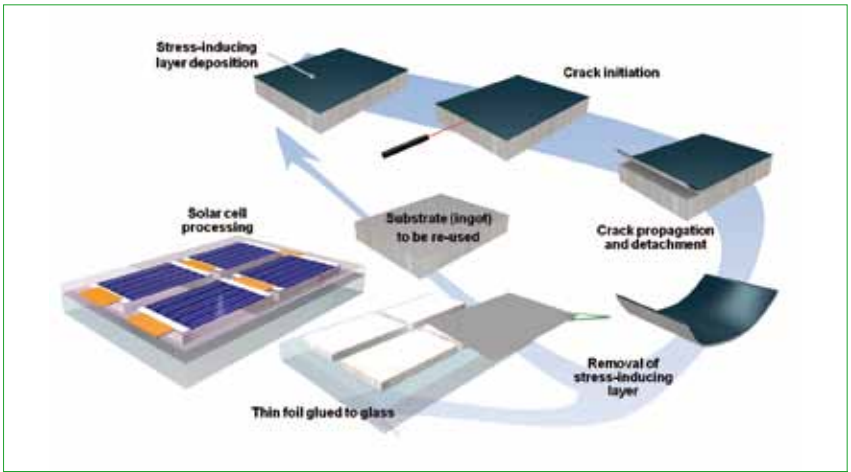


**Figure 2. Schematic of the SLiM-Cut process for the kerf-free fabrication of a c-Si thin foil.**

Several technologies have already been proposed [18], ranging from light-ion implantation [19] and laser wafer-cutting [20], to electrochemical cutting [21] and the stress-induced lift-off method [22]. The stress-induced lift-off (or SLiM-Cut) technique is a kerf-free method investigated at imec, and makes use of a thermomechanically induced crack propagation [22]. A schematic of the process is shown in Fig. 2. A layer of material with a coefficient of thermal expansion (CTE) significantly different from silicon is bonded, at an elevated temperature, on top of a bare silicon substrate. Upon cooling, the stress-inducing layer tends to shrink more than the silicon, giving rise to a stress field inside the silicon substrate. When this stress is higher than the tensile strength of silicon, a fracture occurs, with a spall-off of a thin silicon layer. Under given conditions (material geometries, mechanical properties, process conditions), this fracture can be controlled in terms of depth and direction. The SLiM-Cut development targets a smooth crack path, propagating at a depth of ~50µm, parallel to the original surface.

A proof-of-concept solar cell was fabricated using this material and achieved an efficiency of 10.0% with no intentional texturing and no rear-surface passivation [22]. A crucial requirement for using this material in the c-Si thin-foil concept is the conservation, in the fabricated foil, of the minority-carrier lifetime of the parent substrate. When using metallic stress-inducing layers and a high-temperature process, a complex metallurgic process takes place which explains the excellent adhesion and the thermal stress transferred to the substrate [23]. This process, nonetheless, introduces (metal-decorated) defects, which reduce the minority-carrier lifetime of the sample [24]. From the results of numerical modelling, imec has identified and successfully implemented a polymer material for inducing the stress [25]. The process is metal-free and the temperature remains below 150°C, reducing the chance of contamination and crystal dislocation formation. The material quality is currently being investigated.

## Processing a solar cell on glass

The carpet of silicon foils, obtained either by epitaxy or by a kerf-free wafering method, is then processed at the module level, using the module glass as a mechanical superstrate during processing. For this part of the process, thin-film technologies can be an extensive source of inspiration: light-trapping strategies can be similarly applied, doped layers can be deposited to create rectifying junctions, laser processing can be used for isolation or patterning purposes, large-area metal deposition can be adapted to the needs of the device, etc. The synergies that can be envisaged between thin-film technologies and c-Si thin-foil processing will now be discussed.

Probably the biggest drawback of crystalline silicon for PV application is its low absorption coefficient. Si is an indirect-band-gap semiconductor with, therefore, a smooth absorption edge, leading to only moderate absorption in the near-IR region (600–1200nm). Sunny-side light trapping can be, to a large extent, copied from bulk c-Si technologies. In the case of an epitaxial c-Si thin foil grown on a weak seed layer, the weak layer can be tailored to withstand front-side texturing (e.g. alkaline-based) and antireflection-coating deposition (e.g. PECVD $SiN_x$) [12] – the two main elements in wafer-based light-trapping strategies. Since it has been proved that a two-sided texture can improve the absorption in the active layer, light-management elements can also be placed on the rear [26]. The thin-film community might provide here some elements for solutions [27,28].

In thin-film technologies, the different polarities forming the p-n junction are not diffused, but deposited sequentially. The translation of this principle to the c-Si thin-foil concept implies depositing a material of polarity opposite to the c-Si material to form the junction. One obvious candidate material is a hydrogenated a-Si (a-Si:H) emitter (so-called 'heterojunction'), standardly deposited by PECVD at temperatures below 220°C, compatible with glass. Heterojunction emitters consist of an ultrathin (a few nm) intrinsic a-Si layer, followed by a thin (a few 10nm) doped a-Si layer. This solar cell structure has a high efficiency potential: device efficiencies of up to 23% [29,30,31], and world-record $V_{oc}$s of up to 744mV on 80µm devices have been reported [32]. Since the sunny side is bonded to the glass superstrate, the cell technology will provide both contacts on the rear side. The targeted concept is known as heterojunction-interdigitated back contact (HJ-IBC) and carries all the advantages (and potential) of a back-contact technology [33]. Lately, HJ-IBC technology has been a relatively active field of investigation within several institutes, and the most efficient device, reaching 20.2% efficiency, was recently demonstrated by ISFH and HZB [31]. In the case of an epitaxially-grown active layer, in-situ junction formation for at least one polarity is possible. The epitaxial stack on top of the weak porous-Si layer can consist of, for instance, an emitter, a base of opposite doping type, and a front-surface field.

The common approach nowadays for interconnections of cells in wafer-based technologies involves the build-up of strings of cells already interconnected with Cu-based ribbons. The full strings are then 'gently' grabbed and positioned on the module glass before lamination. The technology is robust and enables module manufacturers to guarantee a lifetime of more than 25 years in the field. Nonetheless, it has the disadvantages of being sequential and barely compatible with very thin cells.

Interconnection of thin-film PV devices is performed directly at the module level. Transparent conductive oxides and/or metals are usually deposited by large-area physical vapour deposition (PVD). The metallization of thin-film c-Si cells mimics the thin-film PV approach based on large-area PVD interconnections: thanks to parallel processing, the complexity and number of steps is reduced [34]. In addition to the parallel-processing possibilities, PVD deposition leads to processing temperatures that are well below 200°C, and is contactless. Moreover, the cells are metallized when already bonded to the final glass superstrate, which alleviates the handling bottleneck of today's technology. Last, but certainly not least, reliability issues are fundamental elements to be mastered before deploying a new module technology involving in particular a novel metallization scheme. They are currently being investigated at imec for this module-level interconnection concept [34,35].

One possible drawback of the concept is the limitation in 'binning' possibilities. In today's mainstream technology, the finished cells are sorted into different classes, and assembled in modules according to their performance. The concept presented here must rely on deposition processes with a particularly high uniformity across the large-area deposition chamber. The risk of mis-processing moves from wafer-to-wafer reproducibility (with binning possibilities) to within-module uniformity.

> "Since the sunny side is bonded to the glass superstrate, the cell technology will provide both contacts on the rear side."

## Evaluation of the efficiency potential

A possible implementation of thin-film-like technologies for c-Si thin-foil devices has been discussed in the previous section. The technology development still faces several challenges, but a careful analysis shows no obvious show-stopper. The most relevant question today is the estimation of the efficiency potential of the technology: in order to justify the technology development and to trigger the paradigm shift, the efficiency potential of the concept has to be (at least) as high as the one achieved with wafer-based crystalline silicon technologies, i.e. above 20%. An assessment of the efficiency potential of the concept is currently being carried out at imec; recent developments are presented next.

High-quality n-type 4-inch FZ 170µm-thick wafers were bonded to a quartz superstrate and a significant part of the process was carried out after the c-Si layer was bonded. Among the different possibilities for creating the c-Si layer, a mimicking of the layer-transfer approach based on epitaxial growth of the active layer was chosen. A schematic of the resulting structure is presented in Fig. 3.

The front side of the bulk wafers was processed free-standing, just like an epitaxial layer would be processed before bonding, while still attached to the mother substrate, as explained previously. Random pyramid texturization was followed by high-temperature passivation, and application of a silicon nitride anti-reflective coating. In addition, the rear-surface diffusion of a p-type emitter was included. Before being bonded, the pre-processed wafer was therefore equivalent to an epitaxial foil based on n-type material, for which the p-type emitter had been epitaxially grown in situ, and the front surface had been processed after epitaxial growth while the thin foil was still mechanically supported by the mother seed-substrate.

The pre-processed wafer was then bonded to a piece of quartz. The chosen bonding material was a silicone developed by Dow Corning for solar cell encapsulation. The rear side of the process occurred on glass, taking into account the processing constraints of glass and encapsulant, such as temperatures below 200°C. The rear-side emitter was patterned (by photolithography), the n+ a-Si back-surface field was deposited by PECVD, and the metallic contact was made by e-beam evaporation.

Table 1 presents the best and average solar cell parameters obtained with the process described above. The best 2cm × 2cm (4cm$^2$ aperture area) device achieves an efficiency of 18.3%. This proves that processing the rear side of a solar cell on glass is compatible with efficiencies exceeding 18%.

A somewhat similar study was carried out by the IPE group in Stuttgart [15], who achieved an efficiency of 16.9% with a front-and-rear-contacted epitaxial foil

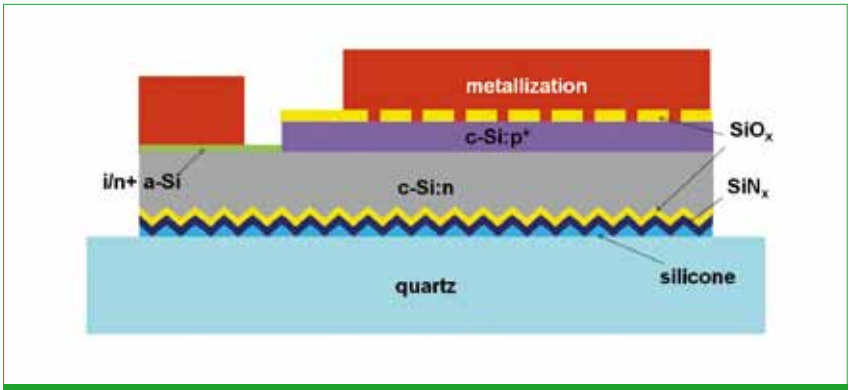


Figure 3. Schematic of the fabricated solar cell device.

having a rear surface partly processed on glass. These results give a lower limit of the potential efficiency of the concept. A careful identification of the sources of losses [36] has led us to believe that the upper efficiency limit has not yet been reached. In fact, the device carries no intrinsic element that drastically reduces its efficiency potential compared to a standard IBC solar cell. The upper limit of the efficiency potential has to be determined in state-of-the-art, free-standing IBC devices reaching efficiencies higher than 23% [37,38,39], and in similar devices based on heterojunctions (and therefore potentially compatible with the constraints of processing on glass), currently achieving efficiencies exceeding 20% [31].

"Starting from pre-processed free-standing monocrystalline wafers bonded to glass, the rear side was processed at a low temperature into an interdigitated contact pattern, and an efficiency exceeding was 18% obtained."

| | $J_{sc}$ [mA/cm$^2$] | $V_{oc}$ [mV] | *FF* [%] | Efficiency [%] | No. of cells |
|---|---|---|---|---|---|
| Average | 36.10 ± 1.42 | 648 ± 7 | 72.0 ± 2.9 | 16.8 ± 1.1 | 16 |
| Best cell | 37.23 | 652 | 75.2 | 18.3 | 1 |

**Table 1. Average and best characteristics of the solar cell devices processed on glass.**

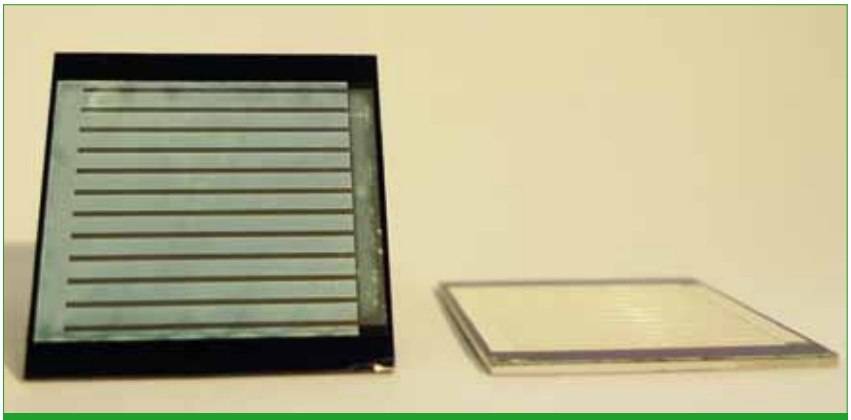

**Figure 4. Picture of the fabricated solar cell device.**

## Conclusion

Today, manufacturers of c-Si wafer-based solar cells cannot reduce the thickness of the starting material, mainly because of mechanical issues. Meanwhile, thin-film producers have absolutely no handling issues, but cannot catch up with the rapidly improving efficiencies of c-Si technologies. Fabricating a carpet of c-Si foils on glass, either by layer transfer of an epitaxially-grown layer or by bonding of a very thin wafer, and processing this c-Si thin-foil device into a photovoltaic module could constitute an advantageous meet-in-the-middle strategy that benefits not only from c-Si material quality but also from thin-film processing developments. How such a device could be envisaged has been discussed; a proof-of-concept and a preliminary estimation of the efficiency potential of the concept have also been presented. Starting from pre-processed free-standing monocrystalline wafers bonded to glass, the rear side was processed at a low temperature into an interdigitated contact pattern, and an efficiency exceeding 18% was obtained.

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